sagantec

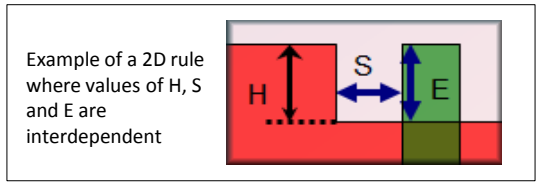
*nm*igrate™
Layout Migration and DRC Correction

Overview
In the world of sub-40nm IC design, as feature size decreases with each new process node, it becomes increasingly difficult to migrate a layout to a new process technology. Too many factors impact manufacturability and yield. At each new process node, to make sure that a given layout is manufacturable and yields well, it is subject to rules that grow in number, type and complexity. Manual migration of a layout from one process technology to another is extremely complex and time-consuming. When an entire library must be migrated, automation is the only practical choice.

Applications
- Process migration
- Foundry re-targeting
- Handling design rule changes
- Creating derivative libraries
- DFM optimization

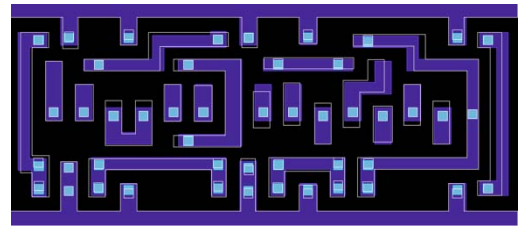
Technology
*nm*igrate is based on 2-D layout optimization technology using dynamic compaction that generates an accurate layout solution optimally satisfying all design rules and constraints. The ability to optimize a layout considering all 2D rules, constraints and cost functions, make it versatile, and suitable for different applications including migration, DRC correction and DFM.

2-D Optimization: The compaction technology allows all 2D rules and effects to be processed in one run, making optimal tradeoffs between constraints and cost in all directions. Including design rules involving multiple shapes where measurement in one dimension influences multiple rule values in the other dimension. Such 2D optimization engine is essential to effectively handle mandatory and DFM rules.



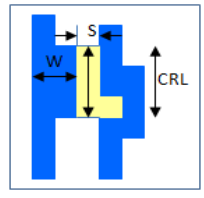
Example of a 2D rule where values of H, S and E are interdependent

Key Features & Benefits
- Automatically delivers 28nm and 20nm DRC-clean layout using 2D optimization
- Most optimal results guaranteed by self-steering and dynamic evaluation engine
- Sophisticated cost function system optimizes layout for yield, variability, reliability and other design metrics
- Supports user-defined constraints and layout templates

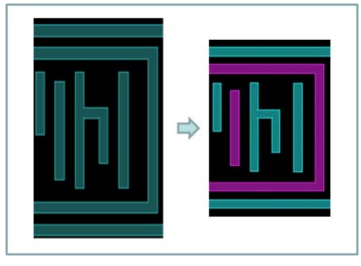

Cell optimized for preferred rules: M1 before/after

Self Steering Dynamic Optimization: Advanced technology design rules may have multiple different and discontinuous correct solutions. When polygons and edges start changing position as part of process migration or DRC correction, finding the optimal solution considering all possible discontinuous position configurations is very difficult and requires an engine that can make the right choices and decisions in a multi-dimensional dynamic environment. *nm*igrate is designed to dynamically evaluate rules and self-steer the engine to achieve the best optimization.

Illustrated are few examples for rules that require dynamic choices and self- steering optimization:



- Width and common run length dependent spacing rule
- Contact groups and via array rules where each spacing value depends on the number and spacing of other shapes.
- Coloring: Due to the printability challenges in 20nm technology new types of rules have been introduced, including DP coloring, A-B spacing rules and auto breaking of odd cycle color conflicts.



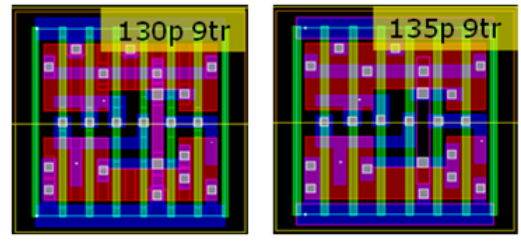
Coloring: showing cell migration from 28nm to 20nm technology. Coloring is done dynamically during compaction

Applications

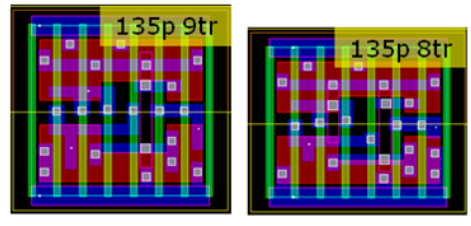
Process Migration: nmigrate can migrate cells and libraries from one technology node to the next one, including 28nm to 20nm migration which requires addressing a host of new rules and challenges, e.g. auto-coloring shown above

Foundry Re-targeting: IC volume and production risk management often require multiple fabrication sources. *nm*igrate automates the process of alternate foundry re-targeting, quickly creating manufacture able layout for the new target foundry.

Design Rule Changes: New process technology rules change often as the process matures. Implementing each such change manually is time-consuming and error-prone. *nm*igrate automates the process and enables quick updates with no time penalty. See below example of a pitch change from 130 to 135nm

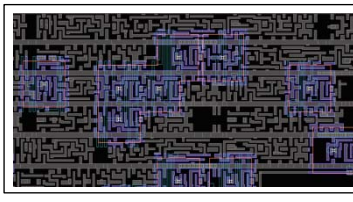


Creating Derivative Libraries: With *nm*igrate, creation of derivative libraries is quick and automated (for example creation of 8-track library from an existing 9-track library).



Full Chip DRC Correction

Often a complete design needs to undergo updates of a few design rules close to tape-out, or even after tape-out for yield enhancement. Similarly, often migrating to a different foundry requires only changing a few design rules. *nm*igrate uses a fast clip-and-fix flow that is completely scalable by using multiple CPUs.



Clip-and-fix: Part of layout showing error locations and clip boundaries

Sagantec North America, Inc.
2075 De La Cruz Blvd. Suite 105
Tel 408.727.6290
Fax 408.727.6288
Email: info@sagantec.com
www.sagantec.com